CLAIMS

1. Electrical impedance tomography (EIT) data processing system, for acquiring and processing data from two-phase flows, comprising a dual-plane sensor, a plurality of digital signal processing modules configured in a data pipeline processing arrangement and a plurality of data acquisition subsystems in communication with a first one of said digital signal processing modules.

2. System as claimed in claim 1 wherein said data acquisition subsystems are in communication with a first one of said digital signal processing modules via a data acquisition interface.

3. System as claimed in claim 1 or claim 2 wherein the data pipeline processing arrangement is capable of acquiring and/or processing 1000 dual frames per second per dual-plane.

4. System as claimed in any of the preceding claims wherein said digital signal processing modules are selectively in communication with a remote PC, preferably via an IEEE1394 interface.

5. System as claimed in any of the preceding claims wherein a first one of said digital signal processing modules is capable of controlling data acquisition and processing.

6. System as claimed in any of the preceding claims wherein a second one of said digital signal processing modules is capable of image reconstruction.

7. System as claimed in any of the preceding claims wherein a third one of said digital signal processing modules is capable of performing velocity calculations by fusing image data to obtain flow information.

8. System as claimed in any of the preceding claims wherein a fourth one of said digital signal processing modules is capable of being configured to carry out additional selected functions.

9. System as claimed in any of the preceding claims further comprising transducers for obtaining conductivity, pressure and/or temperature information, the transducers being in communication with one of said data acquisition subsystems.

10. System as claimed in any of the preceding claims wherein said dual-plane sensor comprises an electrode array in communication with one of said data acquisition subsystems.

11. System as claimed in any of the preceding claims wherein said data acquisition subsystems each include one or more of a voltage controlled current source, an equal-width pulse synthesiser, a synchronised digital demodulation unit and an over-zero switch.

12. System as claimed in claim 11 wherein said voltage controlled current source comprises a parallel structure of eight AD844 chips or equivalents, configured as four pairs in which the two inverting inputs of each pair are cascaded together with a current-setting resistor.

13. System as claimed in claim 12 wherein the four negative current outputs of the AD844 chips are summed together to provide a total negative current output.

14. System as claimed in claim 12 or claim 13 wherein the four positive current outputs are summed together to provide a total positive current output.

15. System as claimed in any of claims 12-14 wherein the voltage controlled current source further comprises a DC restore facility in which a capacitor and a resistor connected to the non-inverting input of each AD844 chip restore DC components and cancel the DC offset at the current outputs.

16. System as claimed in any of claims 12-15 wherein the voltage controlled current source includes a potentiometer for amplitude balancing.

17. System as claimed in any of claims 11-16 wherein said equal-width pulse synthesiser comprises a clock signal for triggering an address generator to continuously output addresses to a pre-programmed memory, the memory output being connected to a digital to analogue converter, the digital to analogue converter providing a staircase signal output, characterised in that different sampling rates are provided at different signal frequencies so that the staircase signal output has the same time step-length at all frequencies.

18. System as claimed in claim 17 wherein said equal-width pulse synthesiser further comprises a low pass filter connected to the output of the digital to analogue converter to provide a smoothed signal output.

19. System as claimed in any of claims 11-18 wherein said synchronised digital demodulation unit comprises 16 sets of programmable gain amplifiers each having an analogue to digital converter, a strobed First-In First-Out (FIFO) memory and control logic.

20. System as claimed in claim 19 wherein the signal output of the equal-width pulse synthesiser triggers said 16 analogue to digital converters to acquire measurement data in parallel at predefined intervals.

21. System as claimed in any of claims 11-20 wherein said over-zero switch comprises two multiplexers, each having 16 electrodes mounted in one sensing plane connected to their 16 output channels and two flip-flops controlled by a switching command from one of said DSP modules.

22. System as claimed in claim 21 wherein said over-zero switch further comprises a D-type flip-flop for preventing data being written prematurely to the second of said flip-flops.

23. Electrical impedance tomography (EIT) data processing system, for acquiring and processing data from two-phase flows, substantially as described herein with reference to any appropriate combination of the accompanying drawings.

24. A method of acquiring and processing electrical impedance tomography data from two-phase flows using the system as claimed in any of the preceding claims.

25. A method of acquiring and processing electrical impedance tomography data from two-phase flows substantially as described herein with reference to any appropriate combination of the accompanying drawings.

26. A recording medium having recorded thereon computer implementable instructions for performing the method of claim 24 or claim 25.